Low Power High Performance Doubletail Comparator

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Abstract—*To**obtain the low power, delay reduction and high performance. In this paper, an analysis on the delay of both conventional dynamic comparator and conventional double tail dynamic comparator which are called clocked regenerative comparator will be presented. Designers can obtain an intuition about the main contributors to the comparator delay and fully explore the trade off in dynamic comparator design. Based on, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low power and fast operation even in small supply voltages. Pre –layout simulation results in a 0.18-µm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. Both delay and power consumption can be reduced by adding few transistors to the proposed comparator. The supply voltage of 0.8 V, while consuming 9µW in modified comparator and 12µW in proposed comparator respectively. Hardware was implemented in FPGA Kit using VHDL coding.***

Keywords—Double tail comparator, low power, fast operation, Pre-layout simulation, and FPGA.

I. Introduction

Comparator is one of the fundamental building blocks in most analog – to –digital converter. Designing high-speed comparators is more challenging when the supply voltage is smaller. In other words to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Developing a new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low voltage operation, especially if they do not increase the circuit complexity. Additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low voltage operation.0.18µm CMOS technology used in tanner software for simulation.C18 process ensuring very low defect densities and high yields.0.18µm CMOS technology offers RF integration, analog mixed signal, digital design flows and high density system on chip capability. The proposed comparator of works down to a supply voltage of 0.8V with a maximum clock frequency consumes 12 µW .Despite the effectiveness of this approach , the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double tail comparator is based on designing a separate input and cross coupled stage. Based on the double tail structure proposed a new dynamic comparator is presented which does not require stacking of too many transistors.By adding a few minimum size transistors to the proposed comparator. Latch delay time and mismatch also reduced. This modification also results in considerable power saving compared to conventional dynamic comparator and double tail comparator. In many applications comparator speed, power dissipation and number of transistors are more important. If comparator speed is priority, the regenerative stage could be designed to start its operation from midway between power supply and ground. There is a wide range of applications for double tail comparator, they are applied in different fields such as operational amplifier, predefined amplifier and analog to digital comparator.it also finds application in sense amplifier. The main advantage of the double tail based latched comparators are their fast speed, low power consumption and adjustable threshold voltage.

II.Material and Methodology

EXISTING SYSTEM

A clocked comparator is a circuit element that makes decision as to whether the input signal is high or low at every clock cycle. Clocked regenerative comparators make fast decision due to strong positive feedback in the regenerative latch. Here analyse the delay of single tail comparator, double tail comparator and proposed comparator.

1.Conventional Single Tail Comparator

The schematic diagram of the conventional dynamic comparator shown in fig 1.1. It widely used in Analog to Digital converter with high input impedance, rail to rail output swing, and no static power consumption.

1.1 Operation

Two modes of operation: Reset Phase and Comparison phase. Block diagram 1.1(a) shows the operation of the comparator. Where $V_{INP} > V_{INN}$, Out_p discharges faster than Out_n.When Out_p (discharged by transistor M_2 drain current), falls down to $V_{DD} - |Vthp|$ before Out_n (discharged by transistor M_1 drain current),the corresponding pMOS transistor (M_5) will turn on initiating the latch regeneration caused by back to back inverters(M_3,M_5 and M_4,M_6). Thus Out_n pulls to V_{DD} and Out_pdischarges to ground. If $V_{INP} < V_{INN}$, the circuits works vice versa. The delay of this comparator is comprised of two time delays ,t_0 and t_{latch}.

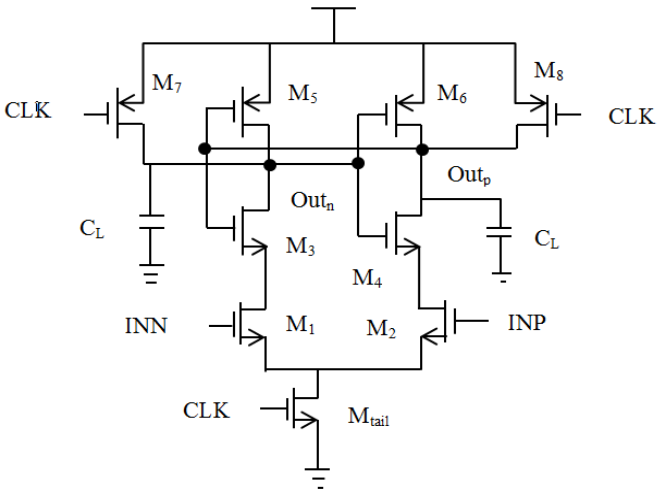
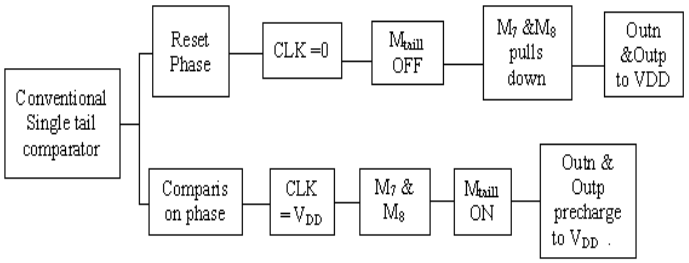


Fig :1.1 Schematic diagram of conventional single tail comparator



Block Diagram: 1.1.1

The delay t_0 represents the capacitive discharge of the load capacitance C_L until the first p channel transistor (M_5/M_6) turn On. The second term,t_{latch} , is the latching delay of two cross coupledinverters. Voltage swing $\Delta V_{out} = V_{DD}/2$ has to be obtained from an initial output voltage difference ΔV_0 at the falling output.

$t_{delay} = t_0+t_{latch}$

2.Conventional Double Tail Comparator

A conventional double tail comparator is shown in fig 2.1. It can operate at lower supply voltages compared to the single tail comparator. The double tail enables both a large current in the latching stage and wider M_{tail2} , for fast latching independent of the input common mode voltage (V_{cm}), and a small current in the input stage (small M_{tail1}), for low offset. Input and ground of the circuit based on the tail current. Intermediate stage transistor is switching when voltage drop occurs at the nodes f_p and fn.

2.1 Operation

Block diagram 2.1.1 shows the operation of double tail comparator. The inter mediate stage formed by M_{R1} and M_{R2} passes $\Delta_{fn/fp}$ to the cross coupled inverters and also provides a good shielding between the input and output, resulting in the reduced value of kickback noise.

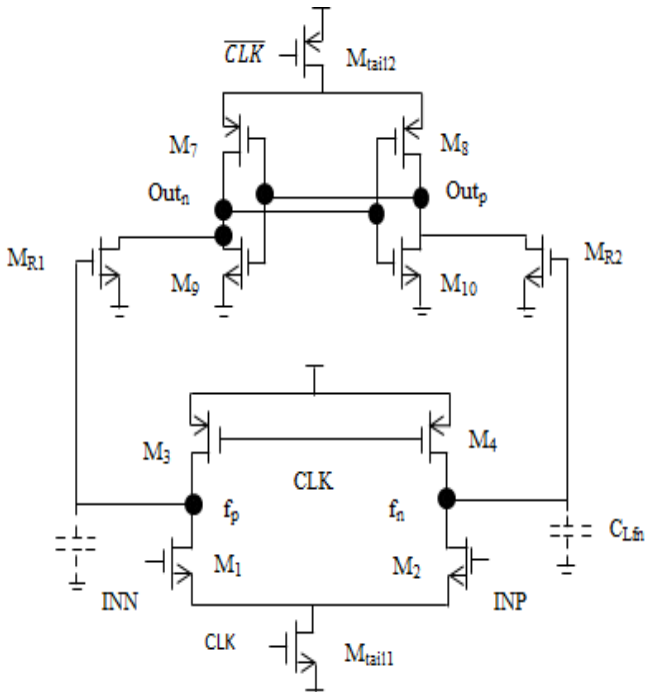
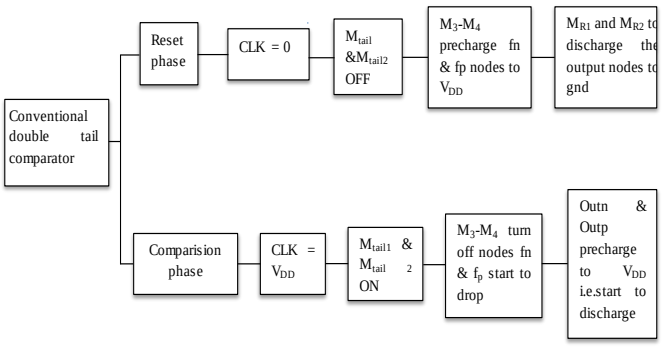


Fig 2.1:Schematic diagram of conventional double tail comparator



Block diagram 2.1.1

3.Proposed Double Tail Dynamic Comparator

Fig 3.1 shows the schematic diagram of the proposed double tail comparator.it gives better performance in low voltage applications, and it is designed based on the double tail structure. Latch regeneration speed is increased by increasing $\Delta V_{fn/fp}$. Two control transistors (M_{C1} and M_{C2}) have been added to the first stage in parallel to M_3/M_4 transistors but in a cross coupled manner for the purpose of increasing speed.

3.1 Operation

During reset phase (CLK=0,M_{tail1} and M_{tail2} are OFF, avoiding static power),M_3 and M_4 pulls both $f_n$and $f_p$nodes to V_{DD},the control transistors are cut off stage.M_{R1} and M_{R2} are Intermediate transistors ,it reset the both latch outputs to ground.

During comparison phase (CLK=V_{DD},M_{tail1} and M_{tail2} are On)transistors M_3 and M_4 turn OFF. twonMOS (M_{sw1} and M_{sw2}) switches used to avoid the static power consumption.

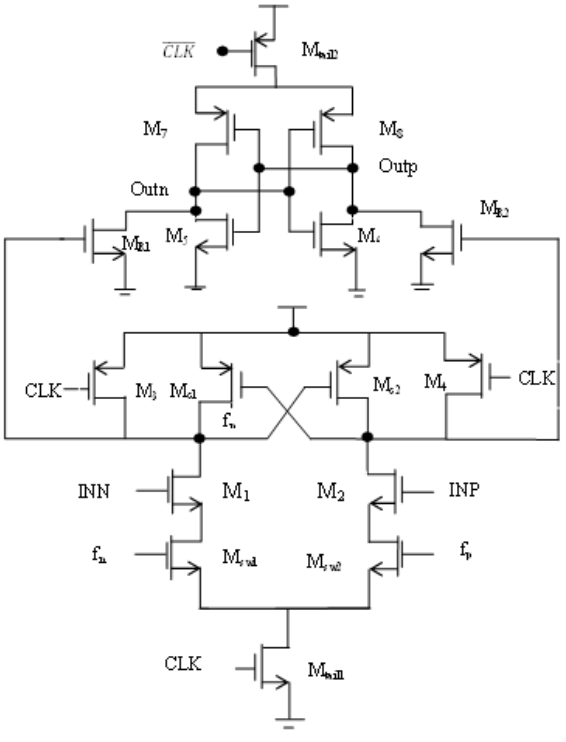


Fig 3.1:schematic diagram of proposed comparator

Proposed comparator enhances the speed of the double tail comparator by affecting two factors such as increases the initial output voltage difference at the beginning of regeneration ($t=t_0$); and it enhances the effective trans conductance.

MODIFICATION

Fig 4 shows the schematic diagram of modified comparator .it is designed based on the proposed comparator.compared with proposed it provides, better performance of double tail comparator in low voltage applications. Drawback of proposed comparator is ,the nodes f_n and f_p starts to drop with different rates according to the input voltages. The continues falling of fn, the corresponding transistor M_{C1} starts to turn on and f_p node backs to V_{DD}. Node fn to be discharged completely(M_{C2} off).When one of the control transistors (M_{C1}) turns ON,a current from V_{DD} is drawn to the ground via input and tail transistor. Resulting a static power consumption. For this purpose two switching transistors (M_{sw3} and M_{sw4}) have been added to M_{sw1} and M_{sw2} in series manner. Modified comparator reduced the delay and power.

4.1.Operation

Operation of modification in both reset and comparison phase is similar as proposed comparator .At the beginning of the decision making phase, both f_n and f_p nodes have been precharged to V_{DD}.in the reset phase switches are closed , f_n and f_p starts to drop with different discharging rates. As soon as comparator detects that one of the f_n/f_p nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Iff$_p$ is pulling up to V_{DD} and f_n should be discharged completely , hence switching in the charging path of f_p will be opened but the other switch connected to f_n will be closedto allow the complete discharge of f_n node. The operation of the control transistors with the switches emulates the operation of the latch.

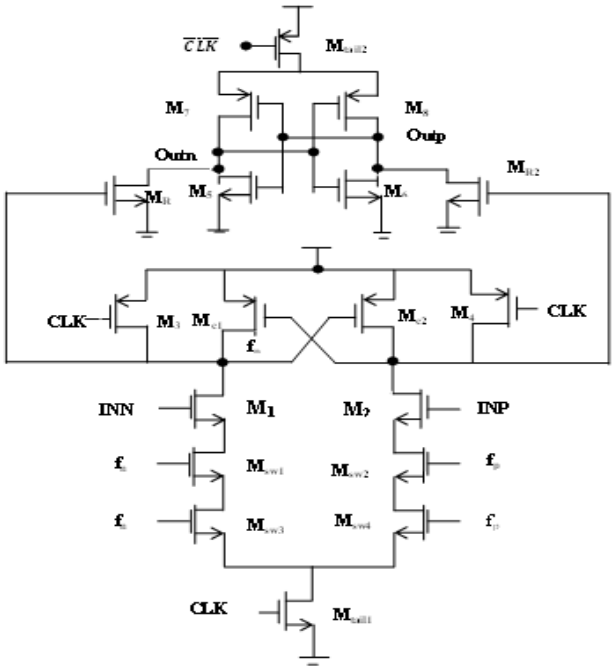


Fig 4 :Schematic diagram of Modified Comparator

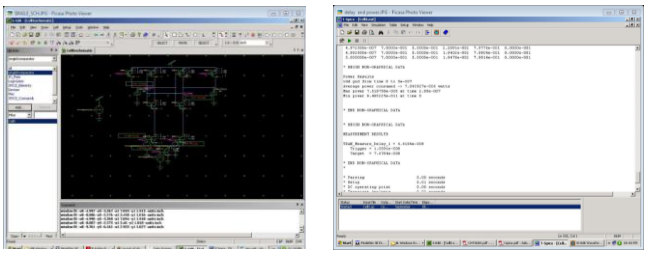
4.2. Design Considerations

The size of transistors can be determined by the time it takes that one of the control transistors turns on must be smaller than t_0(regeneration time).It can be achieved by designing first and second stage of tail currents. Low threshold pMOS devices can be used as control transistors leading to faster turn on in the fabrication technology.another consideration is effect of mismatch between the controlling transistorsof the comparator. Mismatch is a spatial noise spread. In this modification mismatch effect is reduced. The large voltage variations in the internal nodes are coupled to the input disturbing the input voltage called “kick back noise”. Most efficient comparators generate this type of noise. The minimum kickback noise in the double tail comparator.

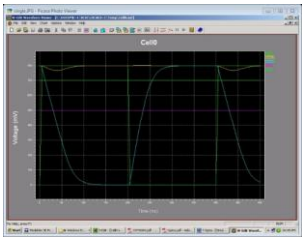
III.Results and Table

Tanner Software (Pre layout simulation)is used for simulation. In order to compare the modified comparator with the Single tail ,double tail and proposed comparators. All circuits have been simulated in a 0.18µm CMOS technology with VDD = 0.8V.The delay of modified comparator is significantly reduced in low voltage supplies. By decreasing the supply voltage, structures are start to behave differently. The double tail comparator can operate faster and can be used in low supply voltages, while consuming nearly the same power as the conventional (single tail) comparator. The case is even better for the modified comparator when compared to the conventional dynamic comparator. Finally table 1 compares the performance of modified comparator with the conventional, double tail and proposed comparator.

A) Conventional (Single Tail)Comparator

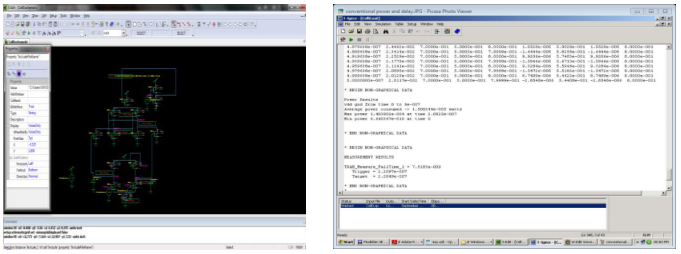


a) Schematic diagramb)Delay and power

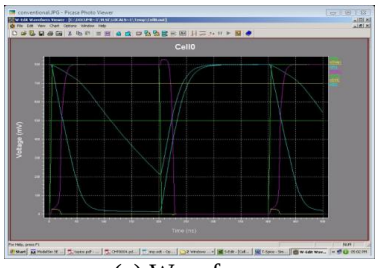


(c) Waveform

B)Double Tail Comparator

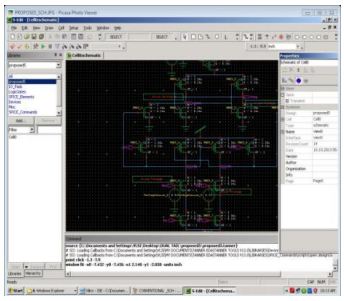


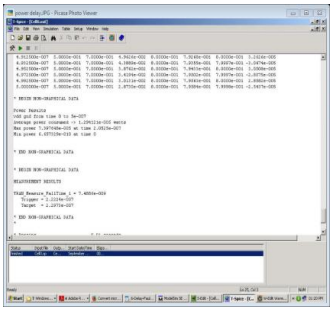
(a) Schematic diagram (b) Delay and Power



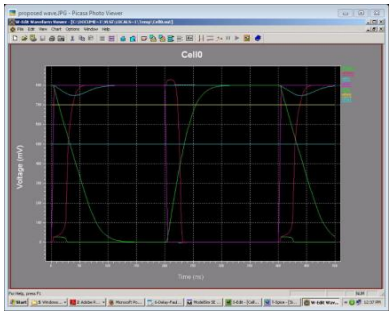
(c) Waveform

C)Proposed Comparator



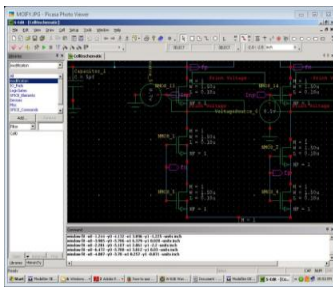


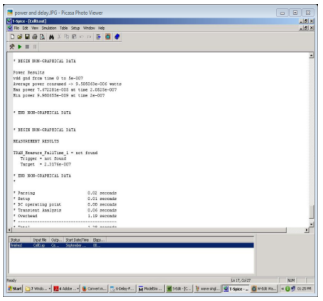
(a) Schematic diagram (b) delay and power



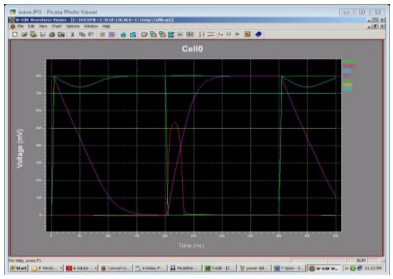
(c) Waveform

D)MODIFIED COMPARATOR





(a) Schematic Diagram (b) Delay and power



(c) Waveform

Performance Comparison Table

Comparator Structure	Conventional Dynamic Comparator	Double Tail Dynamic Comparator	Proposed Dynamic Comparator	Modification
Technology CMOS	180 nm	180 nm	180 nm	180nm
Supply voltage (V)	0.8 V	0.8 V	0.8V	0.8V
Delay	66ns	7.5ns	7.4ns	Not found
Average power	7µ Watts	15µWatts	12µWatts	9µWatts

IV.CONCLUSION

A comprehensive delay analysis of comparator is analysed.A new dynamic comparator with low voltage was proposed in order to improve the performance of the comparator.Pre layout simulation results in 0.18µm CMOS technology confirmed that the delay and energy per conversion of modified comparator is reduced.the table shown the delay of comparator is not found. Hardware implementation is not possible by using tanner software.Instead of tanner Xilinx software is used for implementation. VHDL coding for modified comparator is fetched to the Spartan – 3E FPGA kit. 8bit input is applied to the kit and the output willdisplay on LED. It shows ,which is the high value of input.

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